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(54) **Carrier-to-noise detector for digital transmission systems.**

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Descripti n

BACKGROUND OF THE INVENTION

The present invention relates to a carrier-to-noise detector for digital transmission systems.

The operating performance of the demodulator of a digital transmission system is evaluated by the ratio of per-bit energy to noise (E_b/N_o) of a demodulated digital signal which is defined as:

$$\frac{E_b}{N_o} = \frac{C}{N} \cdot \frac{B}{R}$$

where C/N is a carrier to noise ratio, B, the equivalent noise bandwidth of the demodulator and R, the data transmission rate which is equal to the symbol rate in a 2-PSK system and equal to twice the symbol rate in a 4-PSK system. The C/N ratio is therefore a determining factor for system evaluation. In satellite communications systems, for example, the evaluation of a satellite channel is made by inserting a band-pass filter having a passband narrower than the bandwidth of the satellite transponder at the input of a demodulator. A test carrier having a frequency corresponding to the center frequency of the band-pass filter is transmitted to measure the level of power at the output of the filter which represents the total value (C + N). The carrier is then removed and the power level is again measured as a representation of the noise component N. The carrier component C is then obtained by subtracting the noise N from the total value (C + N) and finally the value C is divided by the noise value N to obtain the ratio C/N. The equivalent noise bandwidth of the band-pass filter corresponds to the constant B.

Because of the manual procedures, the transmission system must be interrupted.

United States Patent US-A-4,124,818 discloses a technique for monitoring signal-to-interference ratio in a radio transmission system, and particularly for channel switching. A bandpass-filtered IF signal is processed to derive a DC component representing the power of the information signal, and a low-frequency component representing the cross-product of the amplitudes of the information signal. A signal-to-interference ratio is obtained by the ratio of the DC component to the cross-product component. When such ratio falls below a predetermined threshold value, switching to an idle channel occurs.

SUMMARY OF THE INVENTION

According to the invention there is provided a carrier-to-noise detector for a digital transmission system, comprising an analog-to-digital converter connected to a demodulator of said digital transmission system for sampling an output signal of said demodulator at a symbol clock rate of said demodulator and converting the sampled signal to a digital output signal having positive and negative values, absolute value converting means for converting said digital output signal from said analog-to-digital converter into a digital signal of an absolute value, first averaging means for averaging said absolute value digital signal over a period of a plurality of symbols sufficient to suppress short term variations, first squaring means for squaring the value of said absolute value digital signal from said first averaging means, second squaring means for squaring the value of the digital signal from said analog-to-digital converter, second averaging means for averaging said squared digital signal from said second squaring means over a period of a plurality of symbols sufficient to suppress short term variations, means for subtracting the squared digital output signal of said first squaring means from the averaged digital output signal of said second averaging means, and means for deriving a ratio between an output of said first squaring means and an output of said subtracting means.

To ensure high precision measurement at high noise levels, the absolute value converting circuit preferably comprises a forward error correcting (FEC) decoder connected to the output of the A/D converter, a forward error correcting encoder connected to the output of the FEC decoder, and a delay circuit for introducing a delay to the output signal of the A/D digital converter by an amount equal to a total of delays introduced by the FEC decoder and encoder. The polarity of the delayed signal is inverted or not inverted depending on the logic states of the output of the FEC encoder before being applied to the first averaging circuit. Alternatively, a weighting circuit is provided for multiplying the absolute value by a weighting factor and applying the weighted value to the first averaging circuit.

The C/N ratio is found to vary with a deviation of the frequency of the carrier recovered by the demodulator from the frequency of the received carrier. The carrier-to-noise ratio detector of the present invention can therefore be used instead of the costly automatic frequency control circuit for preventing the

demodulator from being locked in a pseudo-sync state. This is accomplished by controlling a voltage controlled oscillator provided in a closed loop of the demodulator in accordance with the derived C/N ratio such that the latter is maintained at a maximum level.

BRIEF DESCRIPTION OF THE DRAWINGS

The present invention will be described in further detail with reference to the accompanying drawings, in which:

Fig. 1 is a block diagram of a carrier-to-noise detector according to a first embodiment of the present invention;

Fig. 2 is a circuit diagram of the absolute value circuit of Fig. 1;

Fig. 3 is a circuit diagram of the delay circuit of Fig. 1;

Fig. 4 is a circuit diagram of the C/N ratio divider of Fig. 1;

Fig. 5 is a graphic illustration of the probability density distribution of noise at various noise levels;

Fig. 6 is a graphic illustration of E_b/N_o values measured by the detector of Fig. 1 as a function of input E_b/N_o values for comparison with theoretical E_b/N_o values;

Fig. 7 is a block diagram of the carrier-to-noise ratio detector according to a second embodiment of the invention;

Fig. 8 is a circuit diagram of the polarity inverter of Fig. 6;

Fig. 9 is a graphic illustration of E_b/N_o values measured by the detector of Fig. 7 as a function of input E_b/N_o values for comparison with theoretical E_b/N_o values;

Fig. 10 is a block diagram of the carrier-to-noise detector according to a third embodiment of the present invention;

Fig. 11 is a circuit diagram of the weighting circuit of Fig. 10;

Figs. 12a and 12b are graphic illustrations of the probability density distributions of noise components derived respectively from the outputs of absolute value circuit and weighting circuit of Fig. 10;

Fig. 13 is a graphic illustration of E_b/N_o values measured by the detector of Fig. 10 as a function of input E_b/N_o values for comparison with theoretical E_b/N_o values; and

Fig. 14 is a block diagram of the carrier-to-noise ratio according to a fourth embodiment of the invention.

DETAILED DESCRIPTION

Referring to Fig. 1, there is shown a C/N ratio detector according to a first embodiment of the present invention. The C/N detector comprises an analog-to-digital converter 1 which is connected to receive a demodulated 2-PSK signal from a demodulator, not shown, and driven at a clock rate used to recover symbols by the demodulator for sampling the demodulated signal at the recovered symbol rate. An absolute value circuit 2 is connected to the output of the A/D converter to convert the negative value of the digital output to a positive value and supplies an absolute value signal to a first averaging circuit 3 the output of which is connected to a first squaring circuit 4 to produce an output representing the carrier component value C. The output of A/D converter 1 is further applied to a second squaring circuit 5 to which a second averaging circuit 6 is connected to produce an output representing the total component value (C + N). A subtractor 7 is connected to the outputs of the circuits 4 and 6 to subtract the output of squaring circuit 4 from the output of averaging circuit 6 to obtain the noise component value N. A division circuit 8 is connected to the output of squaring circuit 4 and to the output of the subtractor 7 to determine the ratio C/N.

More specifically, the output of the demodulator is an analog signal having eye patterns at the recovery timing of symbols which corresponds to signal points. A/D converter 1 converts the sampled value into n-bit digital data stream d_i (where i = 0,1,2, ..., n). If n is three, data bit stream d_i can be represented as shown in Table 1. This data bit stream is applied to the absolute value circuit 2 as well as to the second squaring circuit 5.

Absolute value circuit 2 converts the data d_i into an absolute value $| d_i |$. As shown in Fig. 2, the absolute value circuit 2 comprises an n-bit polarity inverter 12 and an $(n+1)$-bit adder 13. If $n=3$, polarity inverter 12 comprises exclusive OR gates 12-1, 12-2 and 12-3 each having a first input terminal connected to the most significant bit (MSB) position output of A/D converter 1 and a second input terminal connected to a respective bit position output of A/D converter 1. The polarity inverter 12 inverts the logic state of the input of each exclusive OR gate when the MSB is at logic *1* and applies the inverted bits to adder 13, while it passes the inputs of all the exclusive OR gates to adder 13 without altering their logic states when the MSB is at logic *0*. Adder 13 adds MSB of the 3-bit inputs from A/D converter 1 to the least significant bit

(LSB) of the 3-bit inputs from the polarity inverter 12 and produces 4-bit outputs. As a result, absolute values shown in Table 2 ar derived.

TABLE 1

	Outputs of A/D Conv. 1
3	011
2	010
1	001
0	000
-1	111
-2	110
-3	101
-4	100

TABLE 2

	Outputs of A.V. Circuit 2
3	0011
2	0010
1	0001
0	0000
1	0001
2	0010
3	0011
4	0100

Averaging circuit 3 averages the absolute values for a period of N symbols which is sufficiently long to suppress short term variations and applies an average value to squaring circuit 4. As shown in Fig. 3, averaging circuit 3 comprises an adder 14 connected to the output of averaging circuit 2, a one-sample delay 15 which is reset at N-symbol intervals and connected between the output of the adder 14 and a second input of the adder 14. Adder 14 and delay 15 form an integrator for integrating N symbols which is divided by a division circuit 16 by a constant N. Since the noise component contained in digital data has a Gaussian distribution centered on an amplitude A at zero noise level, the noise component is cancelled out by the averaging process just described, and therefore, the output of averaging circuit 3 gives the amplitude of a signal point of the demodulated signal under noiseless conditions and is represented by Equation (1).

$$A = \frac{1}{N}\sum_{i=0}^{N-1} |d_i| \quad \cdots\cdots(1)$$

Therefore, the output of squaring circuit 4 supplies a noiseless carrier component C, or the signal power S, which can be represented by:

$$S = A^2 \quad (2)$$

Since the noise component has a Gaussian distribution with respect to the amplitude A at a noiseless signal point, the noise component power σ^2 is given by:

$$\sigma^2 = \frac{1}{N}\sum_{i=0}^{N-1}(|d_i| - A)^2 \quad \cdots\cdots(3)$$

By substituting Equation (1) into Equation (3), the following relation is obtained:

$$\sigma^2 = \frac{1}{N}\sum_{i=0}^{N-1} d_i^2 - A^2 \quad \cdots\cdots(4)$$

On the other hand, the output of A/D converter 1 is squared by second squaring circuit 5 and averaged over N symbols by the second averaging circuit 6 in a manner similar to the processes performed by averaging circuit 3 and squaring circuit 4 just described. As a result, the first term of Equation (4) can be obtained at the output of averaging circuit 6, namely, $\sigma^2 + A^2$. Subtractor 7 subtracts the signal power A^2 at the output of squaring circuit 4 from the $(\sigma^2 + A^2)$ output of averaging circuit 6 to derive a noise power σ^2 which is used by division circuit 8 to divide the output A^2 of squaring circuit 4. As shown in Fig. 4, division circuit 8 comprises a conversion table, or a read only memory 17. A set of values S/σ^2 are stored in cell locations addressable as a function of variables S and σ^2.

Although satisfactory for most applications, the first embodiment is not suited for systems severely affected by noise. As shown in Fig. 5, the probability density distribution of a received 2-PSK signal adopts a curve 40 which is a Gaussian distribution under low noise conditions. Thus, the polarity inversion of the negative values by absolute value circuit 2 causes the signal point with amplitude $-A$ to be folded over to the signal point with amplitude A, while maintaining the symmetry of the curve 40. However, under high noise conditions, there is an increase in variance σ^2 of the Gaussian distribution and the probability density distribution of the received signal adopts a curve as shown at 41. Therefore, the fold-over effect of the absolute value circuit 2 will result in a distribution curve 42 under high noise conditions with the result that the average value of the amplitudes of received signal is shifted to a signal point with an amplitude A'. The amount of this error increases with increase in noise. As shown in Fig. 6, E_b/N_o ratios measured with the circuit of Fig. 1 show increasing discrepancy from theoretical values as the input E_b/N_o ratio decreases.

A second embodiment of the present invention is shown in Fig. 7. This embodiment eliminates the disadvantage of the first embodiment by taking advantage of the forward error coding and decoding techniques employed in digital transmission systems. Instead of using the absolute value circuit 2 of Fig. 1, the second embodiment includes a delay 20 connected to the output of A/D converter 1, an FEC (forward error correcting) decoder 21 for decoding the output of A/D converter 1 and correcting errors and feeding an FEC encoder 22. The output of encoder 22 is connected to one input of a polarity inverter 23 to which the output of delay 20 is also applied. Polarity inverter 23 supplies a decision threshold to the first averaging circuit 3.

FEC decoder 21 performs error decoding operation on the output of A/D converter 1 by correcting errors according to a known error correcting algorithm to generate a signal which is a replica of the original signal prior to application to the FEC encoder of a transmitter, not shown. This signal is applied to FEC encoder 22 in the same way as the transmitter's FEC encoder. With the error decoding and encoding processes, the output of FEC encoder 22 can be considered more akin to the output of the transmitter's FEC encoder than the output of the receiver's demodulator is to it. Therefore, a binary *1* at the output of encoder 22 indicates that the received input signal is at a signal point having an amplitude A in a probability density distribution of amplitudes (Fig. 5) and a binary *0* at the encoder output indicates that the input signal is at a signal point with an amplitude $-A$.

The output of A/D converter 1 is delayed by circuit 20 by an amount equal to the total delay introduced by decoder 21 and encoder 22 so that the inputs to the polarity inverter 23 are rendered time-coincident with each other.

Polarity inverter 23 uses the output of FEC encoder 22 as a criterion to determine whether the output of the delay 20 lies at a signal point having an amplitude A or at a signal point having an amplitude $-A$. In response to a binary *1* from encoder 22, polarity inverter 23 applies the output from delay 20 without altering its polarity to averaging circuit 3 and in response to a binary *0*, it applies the output of delay 20 to

averaging circuit 3 by inverting its polarity. As shown in Fig. 8, polarity inverter 23 comprises a NOT circuit 30 connected to the output of FEC encoder 22, exclusive OR gates 31-*1* to 31-*n*, and an add r 32. Each exclusive OR gate 31 has a first input terminal connected to the output of the NOT circuit 30 and a second input terminal connected to a respective one of the *n* outputs of the delay circuit 20. Since the output of delay 20 is represented by 2's complements of the *n*-bit data, binary *0* at the output of encoder 22 causes the logic states of the outputs of delay 20 to be inverted by exclusive OR gates 31-*1* through 31-*n* and summed with a binary *1* from inverter 30 which is summed by adder 32 with the LSB of the n-bit outputs from exclusive OR gates 31, while a binary *1* at the output of encoder 22 causes the delay 20 outputs to pass through gates 31 to adder 32 without undergoing polarity inversion.

As a result of this polarity inversion process, the probability density distribution of the demodulated signal is centered on the signal point having amplitude *A* and adopts the curve 40 of Fig. 5 and the average value of the amplitudes of the received signal rendered equal to the amplitude at the signal point with amplitude *A*.

In this embodiment, the output of the first squaring circuit 4 can be expressed by the following equation:

$$S = \left(\frac{1}{N} \sum_{i=0}^{N-1} SGN\ (d_i)\, d_i \right)^2 \quad \cdots\cdots\cdots\cdots\cdots\cdots (5)$$

where, $SGN\ (d_i)$ represents the criterion data from FEC encoder 22.

Fig. 9 is a graphic representation of the relationship between the E_b/N_o values obtained by circuit of Fig. 7 and theoretical E_b/N_o values. As is apparent, there is a complete agreement between the measured and theoretical values down to low E_b/N_o input values. This indicates that C/N ratio can be precisely determined even if the transmission system suffers severe noise.

To allow accurate determination of C/N ratio, the use of a powerful error correcting algorithm such as soft decision Viterbi decoding algorithm or convolutional decoding techniques is preferred.

Measurement of C/N ratio of a system without interrupting its service can also be effected alternatively by a third embodiment shown in Fig. 10. This embodiment differs from the first embodiment by the inclusion of a adaptive weighting circuit 50.

Since the probability density distribution of the amplitudes of the received signal adopts a curve A (see Fig. 12a) at low noise levels and a curve B at high noise levels (Fig. 12b), at low noise levels the averaged absolute values of amplitudes becomes approximately equal to the amplitude at the signal point *S*. However, at high noise levels, the averaged absolute values result in an asymmetrical curve C with respect to point *S*.

The absolute value of the output of A/D converter 1 is taken by absolute value circuit 2 and weighted with a prescribed weighting factor by the adaptive weighting circuit 50. Let $S(t)$ represent the signal component of a received signal and $N(t)$ the noise component. Since noise component has a Gaussian distribution, an average value $\overline{N(t)}$ of noise components $N(t)$ can be regarded as being equal to zero, namely $\overline{N(t)} = 0$. The output signal of the adaptive weighting circuit 50 is applied to the first averaging circuit 3 where short term variations, i.e., noise component $N(t)$ are removed to produce an output $\overline{|S(t)|W(u)}$, where $W(u)$ represents the weighting factor, and $u = |S(t) + N(t)|$. Therefore, the output signal of the first squaring circuit 4 is given by $\overline{S(t) \cdot W(u)^2}$. This signal is applied to the subtractor 7 and division circuit 8.

By the squaring and averaging operations by the squaring circuit 5 and the average circuit 6 on the output $\{S(t) + N(t)\}$ of A/D converter 1, the input signal applied from averaging circuit 6 to the subtractor 7 is given by the following relation:

$$\overline{\{S(t)+N(t)\}^2} = \overline{S(t)^2 + N(t)^2 + 2S(t)N(t)}$$
$$= \overline{S(t)^2} + \overline{N(t)^2} + 2\overline{S(t)N(t)} \quad \cdots\cdots (6)$$

Since $\overline{N(t)} = 0$, the third term of Equation (6) becomes zero and so Equation (6) can be rewritten as:

$$\overline{\{S(t) + N(t)\}^2} = \overline{S(t)^2} + \overline{N(t)^2} \qquad (7)$$

This weighting factor is determined so that the adverse fold-over effect produced by taking the absolute values is minimized. The following conditions are examples of weighting factor in which the value x represents the output of the absolute value circuit 2 and TH is a threshold value.

(1) $W(x) = x$

$$(2)\quad W(x) = 1 \quad x > TH$$
$$= 0 \quad x \leq TH$$
$$(3)\quad W(x) = 1 \quad x > TH$$
$$= -\alpha \quad x \leq TH$$

(4) $W(x) = x^2$

Fig. 11 is one example of the adaptive weighting circuit 50 which is constructed according to the condition (3). Weighting circuit 50 comprises a comparator 51, a multiplier 52 and a selector 53 to which the outputs of absolute circuit 2 and multiplier 52 are applied to be selectively coupled to the division circuit 8. Comparator 51 compares between the output of the absolute value circuit 2 and a threshold value TH and applies a logic selection signal to the selector 53. If the output of absolute value circuit 2 is higher than threshold value TH , the selection signal is at logic *1* and if otherwise, the selection signal is at logic *0*. Multiplier 52 multiplies the weighting factor $-\alpha$ on the output of the absolute value circuit 2 and applies it to selector 53. If the comparator 51 output is at logic *1*, the output of absolute value circuit 2 is passed through the selector 52 to the averaging circuit 3 and if otherwise, the output of multiplier 52 is passed to the averaging circuit 3.

Due to the weighting operation, the probability density distribution of the amplitudes of input signal adopts a curve shown at D in Fig. 12b which is shifted to the right from the position of curve C (Fig. 12a) by an amount equal to the distance between the intermediate point 0 and the threshold value *TH*. The weighting factor-α is so determined that the noise component which would otherwise cause the most serious fold-over effect is reduced to a minimum.

Subtractor 7 performs the following subtraction

$$\overline{S(t)^2} + \overline{N(t)^2} - \overline{S(t) \cdot W(u)^2}$$

to produce an output which represents $\overline{N(t)^2}$, which is applied to the division circuit 8. As in the first embodiment, the division circuit 8 comprises a conversion table to which the signals $\overline{N(t)^2}$ and $\overline{S(t)^2} + \overline{N(t)^2}$ are applied as address signals. Fig. 13 is a graphic representation of the characteristic of the third embodiment using a threshold value 0.25, and a weighting factor -0.5. Comparison between Figs. 6 and 13 indicates that precision of the circuit is improved by as much as 4 dB at high noise levels (low E_b/N_o inputs).

The C/N ratio of a demodulator output is found to vary with a deviation of the frequency of the carrier recovered by the demodulator from the frequency of the received carrier. The carrier-to-noise ratio detector of the present invention can therefore be used instead of the costly automatic frequency control circuit for preventing the demodulator from being locked in a pseudo-sync state. This is accomplished by controlling a voltage controlled oscillator provided in a closed loop of the demodulator in accordance with the derived C/N ratio such that the latter is maintained at a maximum level.

As shown in Fig. 14, a pseudo sync detector circuit can be implemented by the C/N ratio detector of the present invention. A demodulator 60 includes a quadrature detector 61 which receives an input PSK signal at terminal 64 and a recovered carrier from a voltage controlled oscillator 62 and produces demodulated signals at terminals 65. The demodulated output signals are applied to a phase detection and filtering circuit 63 to control the VCO 62 in accordance with a phase difference detected between the two output signals. One of the output signals is applied to the input of the C/N ratio detector of the present invention which is identical to that shown in Fig. 1. The output of the division circuit 8 of the C/N ratio detector is applied to a controller 66 including a differential amplifier for comparison with a reference

threshold. This reference threshold corresponds to a DC voltage at which the VCO 62 generates a carrier at the desired frequency when the C/N ratio of the demodulator 60 is at a maxaimum value. The output of the differential amplifier 66 is representative of the deviation of the C/N ratio from its maximum value and is applied to the control terminal of the VCO 62.

When the demodulator is in a sync state, the C/N ratio of the demodulator is at the maximum value. However, if it goes out of sync and enters a pseudo-sync state, the noise component increases in the outputs of the demodulator 60 and hence the C/N ratio of the demodulator decreases, causing the output of the differential amplifier 66 to vary correspondingly. In this way, the VCO frequency is controlled until the output of the division circuit 8 returns to the maximum value of the C/N ratio.

The foregoing description shows only preferred embodiments of the present invention. Various modifications are apparent to those skilled in the art without departing from the scope of the present invention which is only limited by the appended claims.

Claims

1. A carrier-to-noise detector for a digital transmission system, comprising:

an analog-to-digital converter (*1*) connected to a demodulator of said digital transmission system for sampling an output signal of said demodulator at a symbol clock rate of said demodulator and converting the sampled signal to a digital output signal having positive and negative values;

absolute value converting means (*2*) for converting said digital output signal from said analog-to-digital converter into a digital signal of an absolute value;

first averaging means (*3*) for averaging said absolute value digital signal over a period of a plurality of symbols sufficient to suppress short term variations;

first squaring means (*4*) for squaring the value of said absolute value digital signal from said first averaging means;

second squaring means (*5*) for squaring the value of the digital signal from said analog-to-digital converter;

second averaging means (*6*) for averaging said squared digital signal from said second squaring means over a period of a plurality of symbols sufficient to suppress short term variations;

means (*7*) for subtracting the squared digital output signal of said first squaring means from the averaged digital output signal of said second averaging means; and

means (*8*) for deriving a ratio between an output of said first squaring means (*4*) and an output of said subtracting means (*7*).

2. A carrier-to-noise ratio detector as claimed in claim 1, wherein the digital output signal of said analog-to-digital converter is an *n*-bit signal of 2's complement, and wherein said absolute value converting means (*2*) comprises:

a bit inverter (*12*) for inverting the logic states of said *n*-bit outputs of said analog-to-digital converter when the most significant bit thereof is at logic *1* to produce bit-inverted *n*-bit outputs and producing noninverted *n*-bit outputs when said most significant bit is at logic *0*; and

an adder (*13*) for summing said most significant bit to the least significant bit of said bit-inverted and noninverted *n*-bit outputs.

3. A carrier-to-noise detector as claimed in claim 1, wherein said means (*8*) for deriving the ratio comprises a memory (*17*) for storing a plurality of carrier-to-noise ratio values in locations addressable as a function of the outputs of said first squaring means (*4*) and said subtracting means (*7*).

4. A carrier-to-noise ratio detector as claimed in claim 1, wherein said absolute value converting means (*3*) comprises:

a forward error correcting decoder (*21*) connected to the output of said analog-to-digital converter (*1*);

a forward error correcting encoder (*22*) connected to the output of said forward error correcting decoder (*21*);

a delay circuit (*20*) for introducing a delay to the output signal of said analog-to-digital converter (*1*) by an amount equal to a total of delays introduced by said forward error correcting decoder (*21*) and encoder (*22*); and

a polarity inverter (*23*) for inverting the polarity of the output of said delay circuit depending on the logic state of the output of said forward error correcting encoder (*22*) to supply the polarity inverted

output to said first averaging means and supplying the output of said delay circuit without inverting the polarity thereof to said first averaging circuit.

5. A carrier-to-noise ratio detector as claimed in claim 4, wherein the digital output signal of said analog-to-digital converter is an *n*-bit signal of 2's complement, and wherein said polarity inverter (*23*) comprises:

a bit inverter (*31*) for inverting the logic states of the output of said delay circuit or not inverting said logic states depending on the logic state of the output of said encoder (*22*); and

an adder (*32*) for summing the output of said encoder (*22*) to the least significant bit of said inverted and noninverted *n*-bit outputs from said bit inverter (*31*).

6. A carrier-to-noise ratio detector as claimed in claim 1, further comprising weighting means (*50*) for multiplying said absolute value digital signal by a weighting factor and applying the weighted digital signal to said first averaging means (*3*).

7. A carrier-to-noise ratio detector as claimed in claim 6, wherein said weighing means (*50*) comprises:

a comparator (*51*) for comparing said absolute value digital signal with a reference value and producing a first switching control signal when said absolute value digital signal is higher than said reference value and a second switching signal when said absolute value digital signal is lower than said reference value;

a multiplier (*52*) for multiplying said weighting factor on said absolute value digital signal; and

a selector (*53*) for applying said absolute value digital signal to said first averaging means (*3*) in response to said first switching control signal and applying an output of said multiplier to said first averaging circuit in response to said second switching signal.

8. A carrier-to-noise detector as claimed in claim 1, wherein said demodulator includes a voltage controlled oscillator (*62*) for recovering a carrier as a replica of the carrier of a received signal, further comprising means (*66*) responsive to said ratio deriving means (*8*) for controlling the output frequency of said voltage controlled oscillator such that said ratio deriving means produces an output of a maximum level.

Patentansprüche

1. Träger/Rausch-Detektor für ein digitales Übertragungssystem mit:

einem Analog/Digital-Wandler (1), der mit einem Demodulator des digitalen Übertragungssystems verbunden ist, um ein Ausgangssignal des Demodulators mit einer Zeichentaktrate des Demodulators abzutasten und das abgetastete Signal in ein digitales Ausgangssignal mit positiven und negativen Werten zu wandeln;

einer Absolutwert-Wandlereinrichtung (2), um das digitale Ausgangssignal des Analog/Digital-Wandlers in ein digitales Signal mit einem Absolutwert zu wandeln;

einer ersten Mittelungseinrichtung (3), um das digitale Absolutwertsignal über eine Periode mehrerer Zeichen zu mitteln, die ausreicht, kurzeitige Schwankungen zu unterdrücken;

einer ersten Quadrierungseinrichtung (4), um den Wert des digitalen Absolutwertsignals aus der ersten Mittelungseinrichtung zu quadrieren;

einer zweiten Quadrierungseinrichtung (5), um den Wert des digitalen Signals aus dem Analog/Digital-Wandler zu quadrieren;

einer zweiten Mittelungseinrichtung (6), um das quadrierte digitale Signal aus der zweiten Quadrierungseinrichtung über eine Periode mehrerer Zeichen zu mitteln, die ausreicht, kurzeitige Schwankungen zu unterdrücken;

einer Einrichtung (7), um das quadrierte digitale Ausgangssignal aus der ersten Quadrierungseinrichtung von dem gemittelten digitalen Ausgangssignal aus der zweiten Mittelungseinrichtung zu subtrahieren; und

einer Einrichtung (8), um ein Verhältnis zwischen einem Ausgangssignal aus der ersten Quadrierungseinrichtung (4) und einem Ausgangssignal aus der Subtraktionseinrichtung (7) abzuleiten.

2. Träger/Rausch-Verhältnisdetektor nach Anspruch 1, bei dem das digitale Ausgangssignal des Analog/Digital-Wandlers ein n-Bit Zweier-Komplement-Signal ist, und bei dem die Absolutwert-Wandlereinrichtung (2) aufweist:

einen Bitinverter (12), um die logischen Zustände der n-Bit-Ausgangssignale des Analog/Digital-Wandlers zu invertieren, wenn sich dessen höchstwertiges Bit auf logisch "1" befindet, um bitinvertierte n-Bit-Ausgangssignale zu erzeugen, und um nicht bitinvertierte n-Bit-Ausgangssignale zu erz ugen, wenn sich das das höchstwertige Bit auf logisch "0" befindet; und

einen Addierer (13), um das höchstwertige Bit auf das niedervertigste Bit der bitinvertierten und der nicht invertierten n-Bit-Ausgangssignale zu summieren.

3. Träger/Rausch-Detektor nach Anspruch 1, bei dem die Einrichtung (8) zur Ableitung des Verhältnisses einen Speicher (17) aufweist, um mehrere Träger/Rausch-Verhältniswerte an Stellen abzuspeichern, die als Funktion der Ausgangssignale der ersten Quadrierungseinrichtung (4) und der Subtrahiereinrichtung (7) adressierbar sind.

4. Träger/Rausch-Verhältnisdetektor nach Anspruch 1, bei dem die Absolutwert-Wandlereinrichtung (3) aufweist:

einen mit dem Ausgang des Analog/Digital-Wandlers (1) verbundenen Vorwärtsfehler-Korrekturdekoder (21);

einen mit dem Ausgang des Vorwärtsfehler-Korrekturdekoders (21) verbundenen Vorwärtsfehler-Korrekturkodierer (22);

eine Verzögerungsschaltung (20), um eine Verzögerung in das Ausgangssignal des Analog/Digital-Wandlers (1) um einen Betrag einzuführen, der gleich dem durch die Vorwärtsfehler-Korrekturdekoder (21) und Kodierer (22) eingeführten Gesamtverzögerungen ist; und

einen Polaritätsinverter (23), um die Polarität des Ausgangssignals der Verzögerungsschaltung in Abhängigkeit von dem logischen Zustand des Ausgangssignals des Vorwärtsfehlerkodierers (22) zu invertieren, um das polaritätsinvertierte Ausgangssignal an die erste Mittelungseinrichtung zu liefern, und um das Ausgangssignal der Verzögerungsschaltung ohne Invertierung von dessen Polarität an die erste Mittelungseinrichtung zu liefern.

5. Träger/Rausch-Verhältnisdetektor nach Anspruch 4, bei dem das digitale Ausgangssignal des Analog/Digital-Wandlers ein n-Bit Zweier-Komplement-Signal ist, und bei dem der Polaritätsinverter (23) aufweist:

einen Bitinverter (31), um die Logikzustände des Ausgangssignals der Verzögerungsschaltung zu invertieren oder die Logikzustände, abhängig vom logischen Zustand des Ausgangssignals des Kodierers (22), nicht zu invertieren; und

einen Addierer (32), um das Ausgangssignal des Kodierers (22) auf das niederwertigste Bit der invertierten oder nichtinvertierten Ausgangssignale aus dem Bitinverter (31) zu addieren.

6. Träger/Rausch-Verhältnisdetektor nach Anspruch 1, der ferner eine Wichtungseinrichtung (50) aufweist, um das digitale Absolutwertsignal mit einem Wichtungsfaktor zu multiplizieren und das gewichtete Digitalsignal an die erste Mittelungseinrichtung (3) anzulegen.

7. Träger/Rausch-Verhältnisdetektor nach Anspruch 6, bei dem die Wichtungseinrichtung (50) aufweist:

einen Komparator (51), um das digitale Absolutwertsignal mit einem Referenzsignal zu vergleichen und um ein erstes Schaltsteuersignal zu erzeugen, wenn das digitale Absolutwertsignal höher als das Referenzsignal ist, und um ein zweites Schaltsteuersignal zu erzeugen, wenn das digitale Absolutwertsignal niedriger als das Referenzsignal ist;

einen Multiplizierer (52), um den Wichtungsfaktor mit dem digitalen Absolutwertsignal zu multiplizieren; und

einen Auswahlschalter (53), um das digitale Absolutwertsignal als Antwort auf das erste Schaltsteuersignal an die erste Mittelungseinrichtung (3) anzulegen, und um ein Ausgangssignal des Multiplizierers als Antwort auf das zweite Schaltsteuersignal an die erste Mittelungseinrichtung anzulegen.

8. Träger/Rausch-Detektor nach Anspruch 1, bei dem der Demodulator einen spannungsgesteuerten Oszillator (62) enthält, um einen Träger als Nachbildung des Trägers eines empfangenen Signals wiederherzustellen, und der ferner eine auf die Verhältnisableitungseinrichtung (8) reagier nde Einrichtung (66) aufweist, um die Ausgangsfrequenz des spannungsgesteuerten Oszillators in der Weise zu steuern, daß die Verhältnisableitungseinrichtung ein Ausgangssignal mit maximalen Pegel erzeugt.

Revendications

1. Détecteur du rapport porteuse/bruit pour un système de transmission numérique, comprenant:
un convertisseur analogique/numérique (1) connecté à un démodulateur dudit système de transmission numérique pour échantillonner un signal de sortie dudit démodulateur à une fréquence de base de symboles dudit démodulateur et convertir le signal échantillonné en un signal de sortie numérique ayant des valeurs positive et négative;
un moyen de conversion en valeur absolue (2) pour convertir ledit signal de sortie numérique provenant dudit convertisseur analogique/numérique en un signal numérique d'une valeur absolue;
un premier moyen d'établissement de moyenne (3) pour établir la moyenne dudit signal de sortie de valeur absolue sur une période d'une pluralité de symboles suffisant à supprimer les variations à court terme;
un premier moyen d'élévation au carré (4) pour élever au carré la valeur dudit signal numérique de valeur absolue provenant dudit premier moyen d'établissement de moyenne;
un deuxième moyen d'élévation au carré (5) pour élever au carré la valeur du signal numérique provenant dudit convertisseur analogique/numérique;
un deuxième moyen d'établissement de moyenne (6) pour établir la moyenne dudit signal numérique élevé au carré provenant dudit deuxième moyen d'élévation au carré sur une période d'une pluralité de symboles suffisant à supprimer les variations à court terme;
un moyen (7) pour soustraire le signal de sortie numérique élevé au carré dudit premier moyen d'élévation au carré du signal de sortie numérique moyen dudit deuxième moyen d'établissement de moyenne; et
un moyen (8) pour dériver un rapport entre une sortie dudit premier moyen d'élévation au carré (4) et une sortie dudit moyen de soustraction (7).

2. Détecteur du rapport porteuse/bruit selon la revendication 1, dans lequel le signal de sortie numérique dudit convertisseur analogique/numérique est un signal à n bits de complément à 2, et dans lequel ledit moyen de conversion en valeur absolue (2) comprend:
un inverseur de bits (12) pour inverser les états logiques desdites sorties de n bits dudit convertisseur analogique/numérique quand le bit de poids fort de celles-ci est au 1 logique pour produire des sorties de n bits à bits inversés et produire des sorties de n bits non inversés quand ledit bit de poids fort est au 0 logique; et
un circuit additionneur (13) pour additionner ledit bit de poids fort au bit de poids faible desdites sorties de n bits à bits inversés et à bits non inversés.

3. Détecteur du rapport porteuse/bruit selon la revendication 1, dans lequel ledit moyen (8) pour dériver le rapport comprend une mémoire (17) pour mémoriser une pluralité de valeurs de rapports de porteuse/bruit à des emplacements adressables en fonction des sorties dudit premier moyen d'élévation au carré (4) et dudit moyen de soustraction (7).

4. Détecteur du rapport porteuse/bruit selon la revendication 1, dans lequel ledit moyen de conversion en valeur absolue (3) comprend:
un décodeur de correction d'erreurs sans voie de retour (21) connecté à la sortie dudit convertisseur analogique/numérique (1);
un codeur de correction d'erreurs sans voie de retour (22) connecté à la sortie dudit décodeur de correction d'erreurs sans voie de retour (21);
un circuit de temporisation (20) pour introduire une temporisation du signal de sortie dudit convertisseur analogique/numérique (1) d'un montant égal à un total de temporisations introduites par lesdits décodeur (21) et codeur (22) de correction d'erreurs sans voie de retour; et
un inverseur de polarité (23) pour inverser la polarité de la sortie dudit circuit de temporisation en fonction de l'état logique de la sortie dudit codeur de correction d'erreurs sans voie de retour (22) pour fournir la sortie à polarité inversée audit premier moyen d'établissement de moyenne et fournir la sortie dudit circuit de temporisation sans en inverser la polarité audit premier circuit d'établissement de moyenne.

5. Détecteur du rapport porteuse/bruit selon la revendication 4, dans lequel le signal de sortie numérique dudit convertisseur analogique/numérique est un signal à n-bits de complément à 2, et dans lequel ledit inverseur de polarité (23) comprend:

un inverseur de bits (31) pour inverser les états logiques de la sortie dudit circuit de temporisation ou ne pas inverser lesdits états logiques en fonction de l'état logique de la sortie dudit codeur (22); et

un circuit additionneur (32) pour additionner la sortie dudit codeur (22) au bit de poids faibl desdites sorties de n bits à bits inversés et à bits non inversés provenant dudit inverseur de bits (31).

6. Détecteur du rapport porteuse/bruit selon la revendication 1, comprenant en outre un moyen de pondération (50) pour multiplier ledit signal numérique de valeur absolue par un facteur de pondération et appliquer le signal numérique pondéré audit premier moyen d'établissement de moyenne (3).

7. Détecteur du rapport porteuse/bruit selon la revendication 6, dans lequel ledit moyen de pondération (50) comprend:

un comparateur (51) pour comparer ledit signal numérique de valeur absolue avec une valeur de référence et produire un premier signal de contrôle de commutation lorsque ledit signal numérique de valeur absolue est supérieur à ladite valeur de référence et un deuxième signal de commutation lorsque ledit signal numérique de valeur absolue est inférieur à ladite valeur de référence;

un circuit de multiplication (52) pour multiplier ledit facteur de pondération sur ledit signal numérique de valeur absolue; et

un sélecteur (53) pour appliquer ledit signal numérique de valeur absolue audit premier moyen d'établissement de moyenne (3) en réponse audit premier signal de contrôle de commutation et appliquer une sortie dudit circuit de multiplication audit premier circuit d'établissement de moyenne en réponse audit deuxième signal de commutation.

8. Détecteur du rapport porteuse/bruit selon la revendication 1, dans lequel ledit démodulateur comporte un oscillateur commandé en tension (62) pour récupérer une porteuse réplique de la porteuse d'un signal reçu, comprenant en outre un moyen (66) répondant audit moyen de dérivation de rapport (8) pour contrôler la fréquence de sortie dudit oscillateur commandé en tension de sorte que ledit moyen de dérivation de rapport produit une sortie d'un niveau maximum.

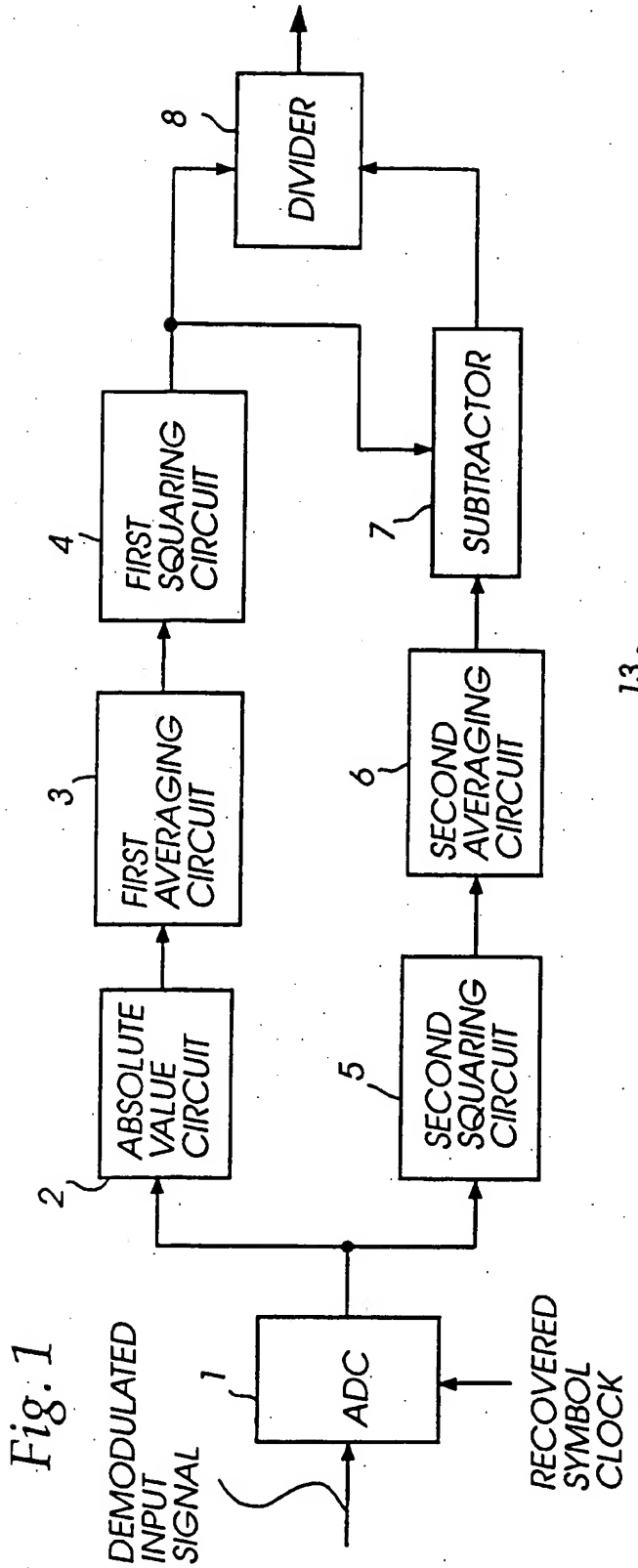

DEMODULATED INPUT SIGNAL
1
ADC
RECOVERED SYMBOL CLOCK
2
ABSOLUTE VALUE CIRCUIT
3
FIRST AVERAGING CIRCUIT
4
FIRST SQUARING CIRCUIT
5
SECOND SQUARING CIRCUIT
6
SECOND AVERAGING CIRCUIT
7
SUBTRACTOR
8
DIVIDER

Fig. 1

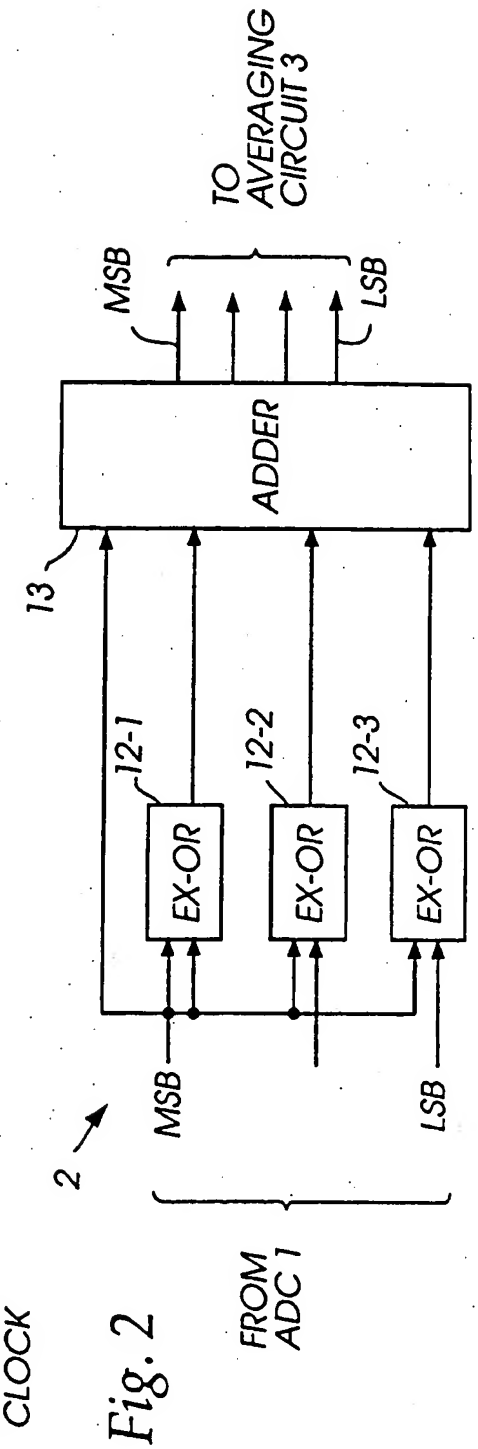

FROM ADC 1
2
MSB
LSB
12-1
12-2
12-3
EX-OR
EX-OR
EX-OR
13
ADDER
MSB
LSB
TO AVERAGING CIRCUIT 3

Fig. 2

Fig. 3

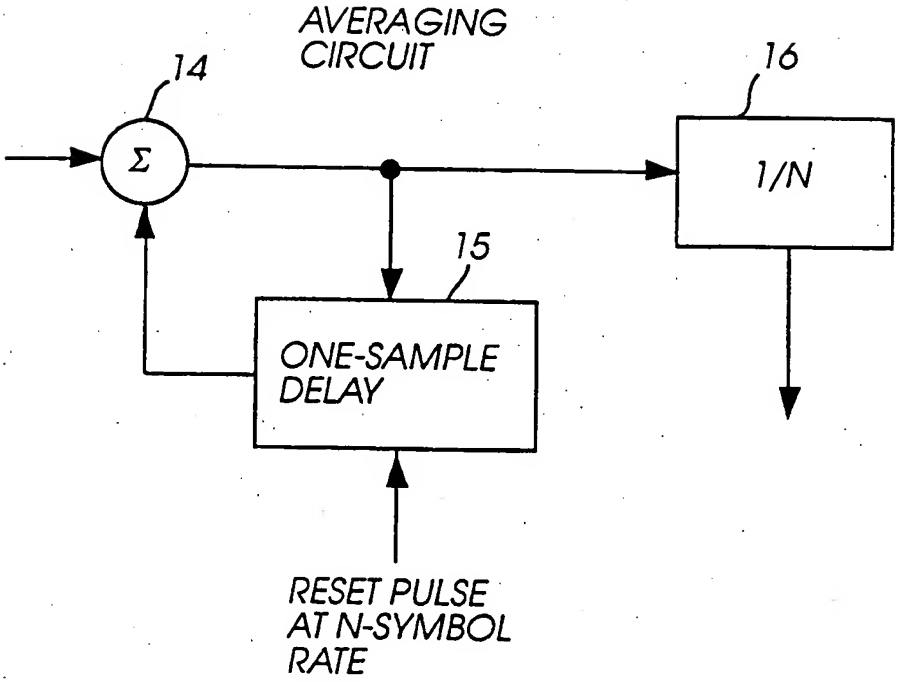

AVERAGING CIRCUIT
14
16
Σ
1/N
15
ONE-SAMPLE DELAY
RESET PULSE AT N-SYMBOL RATE

Fig. 4

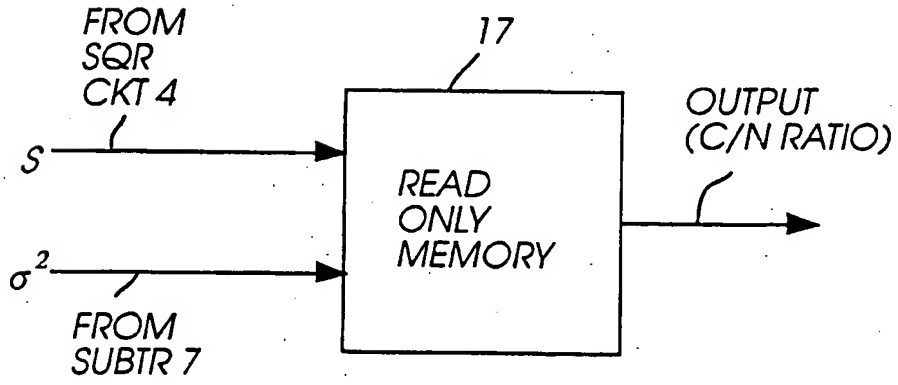

FROM SQR CKT 4
17
S
OUTPUT (C/N RATIO)
READ ONLY MEMORY
σ²
FROM SUBTR 7

Fig. 5

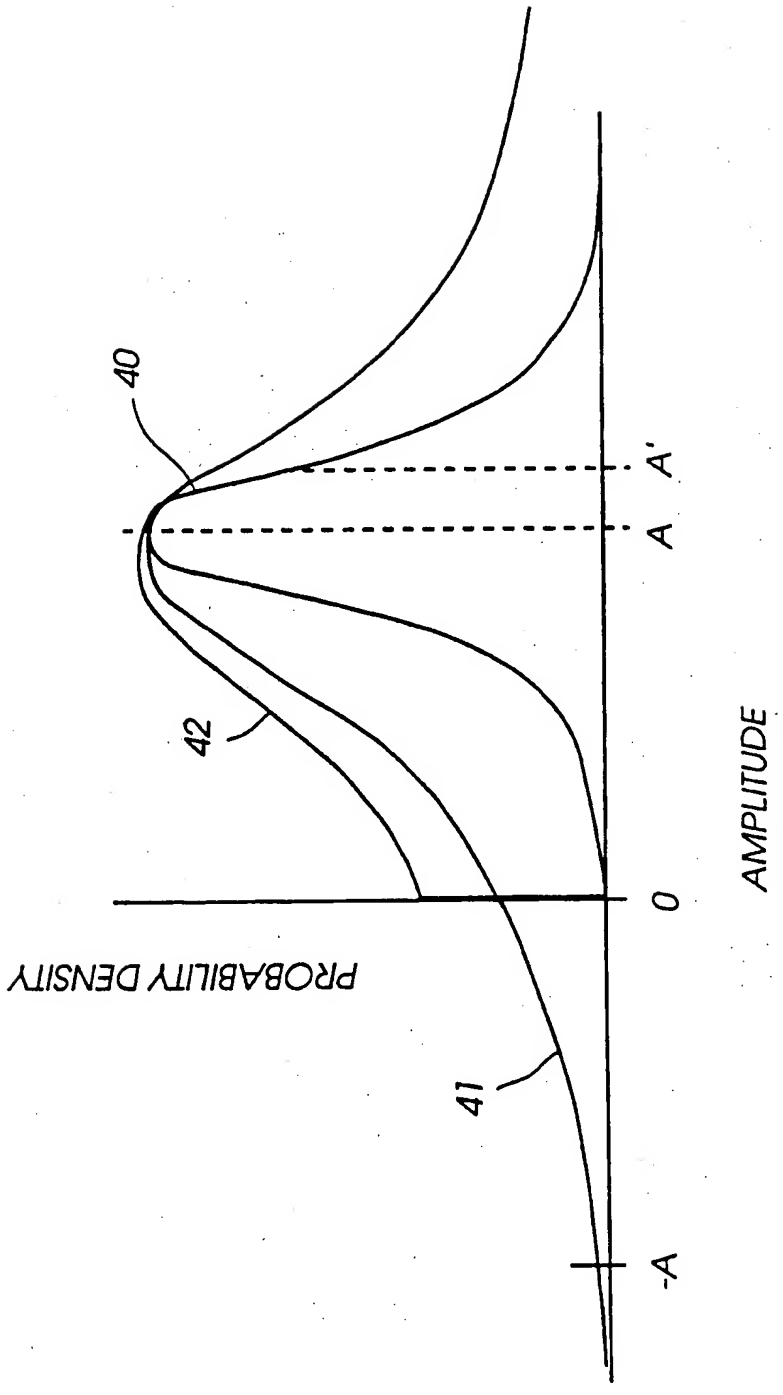
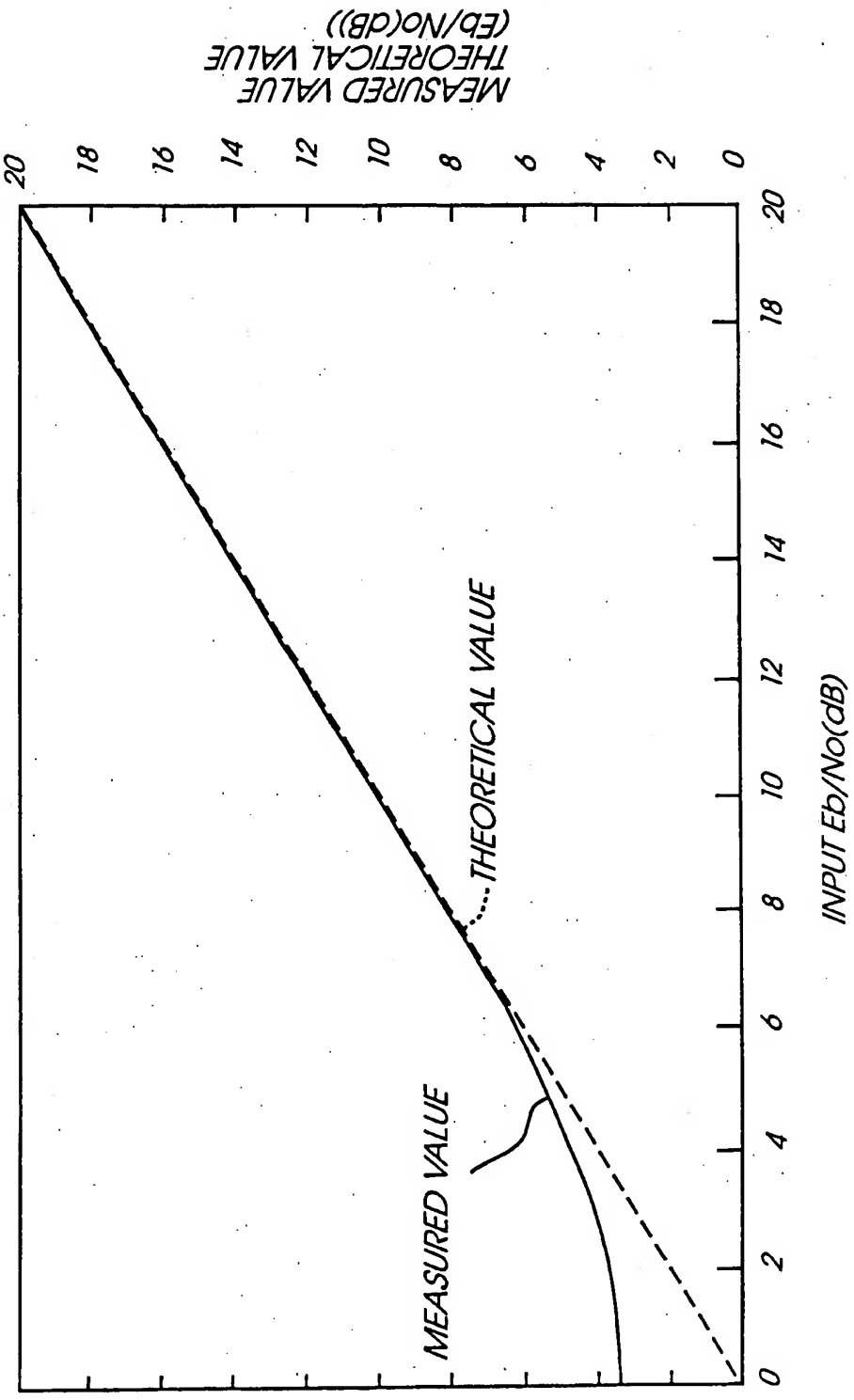


Fig. 6


MEASURED VALUE
THEORETICAL VALUE (Eb/No(dB))
INPUT Eb/No(dB)
THEORETICAL VALUE
MEASURED VALUE
0
2
4
6
8
10
12
14
16
18
20

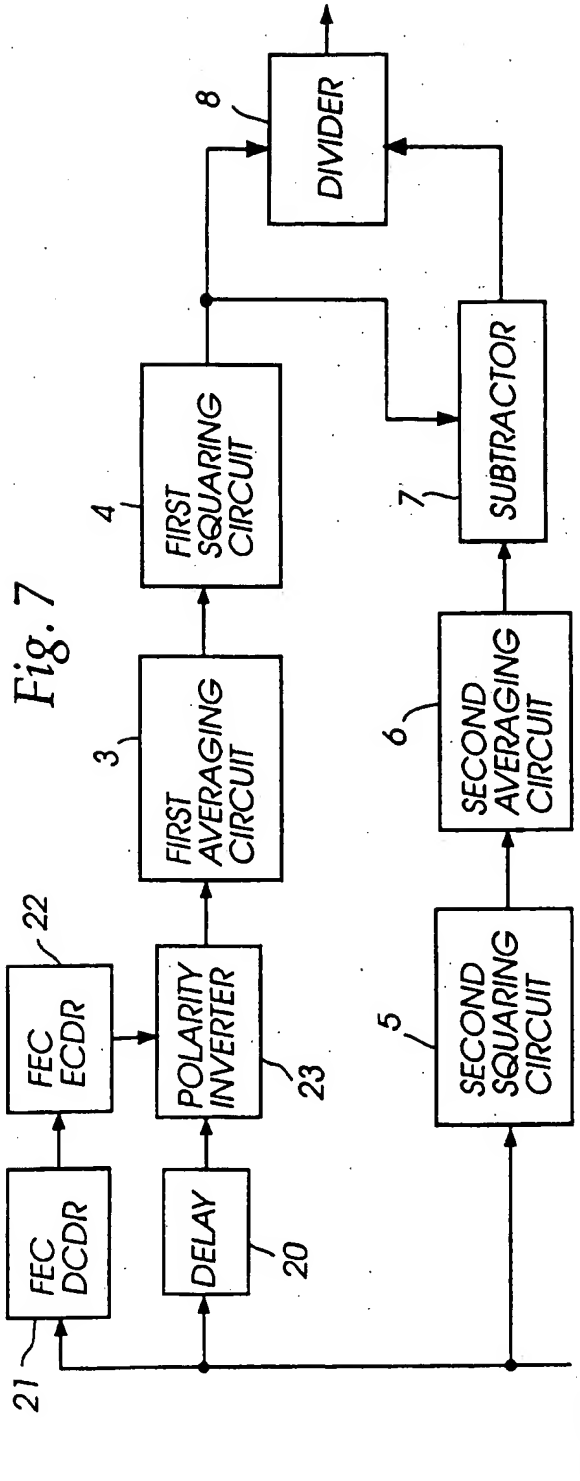

FROM A/D CONV. 1
21
FEC DCDR
DELAY
20
FEC ECDR
22
POLARITY INVERTER
23
FIRST AVERAGING CIRCUIT
3
FIRST SQUARING CIRCUIT
4
DIVIDER
8
5
SECOND SQUARING CIRCUIT
6
SECOND AVERAGING CIRCUIT
7
SUBTRACTOR

Fig. 7

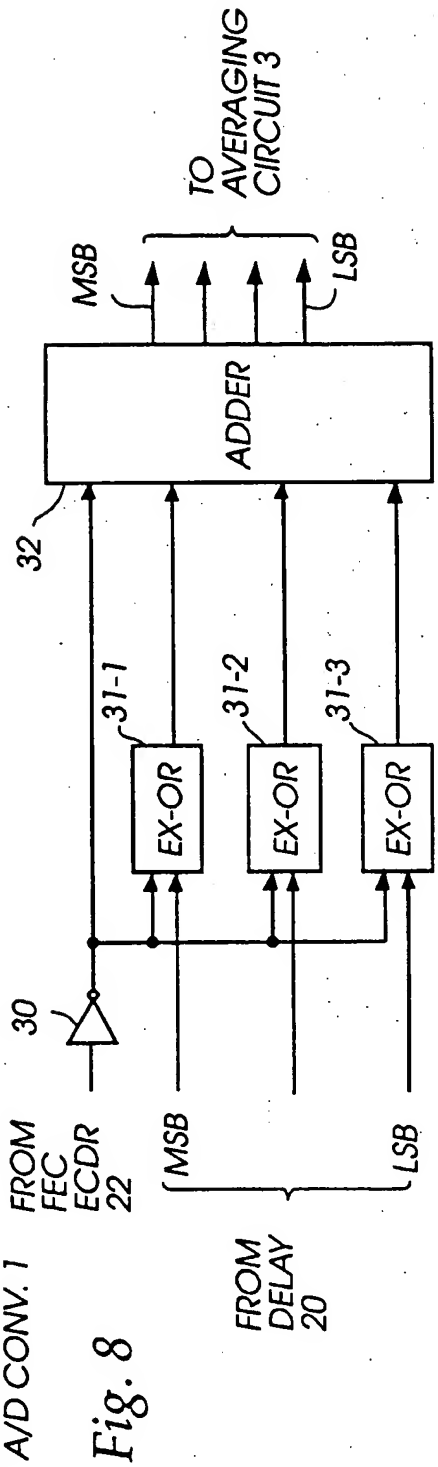

FROM FEC ECDR 22
FROM DELAY 20
30
MSB
LSB
31-1
31-2
31-3
EX-OR
EX-OR
EX-OR
32
ADDER
MSB
LSB
TO AVERAGING CIRCUIT 3

Fig. 8

Fig. 9

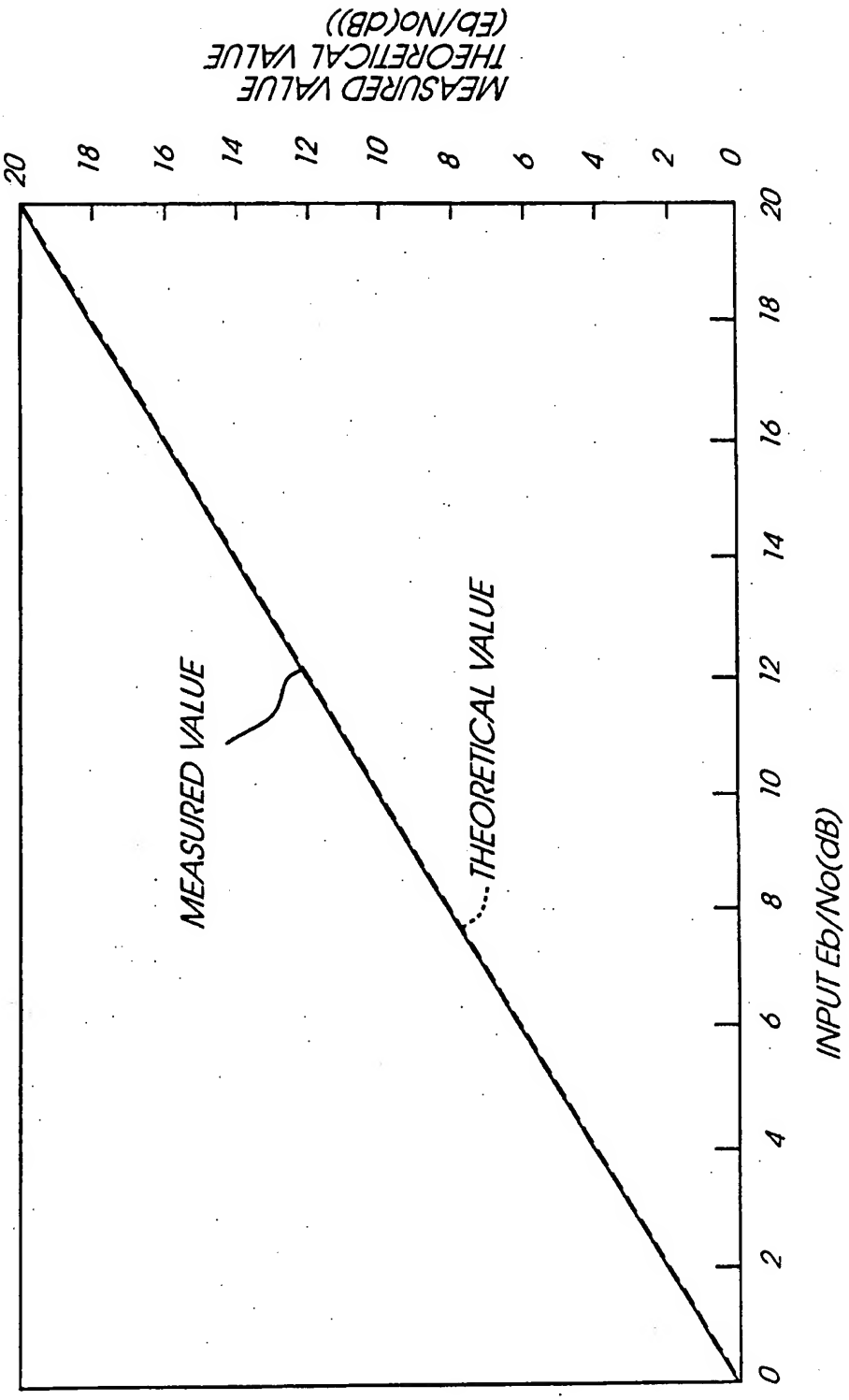
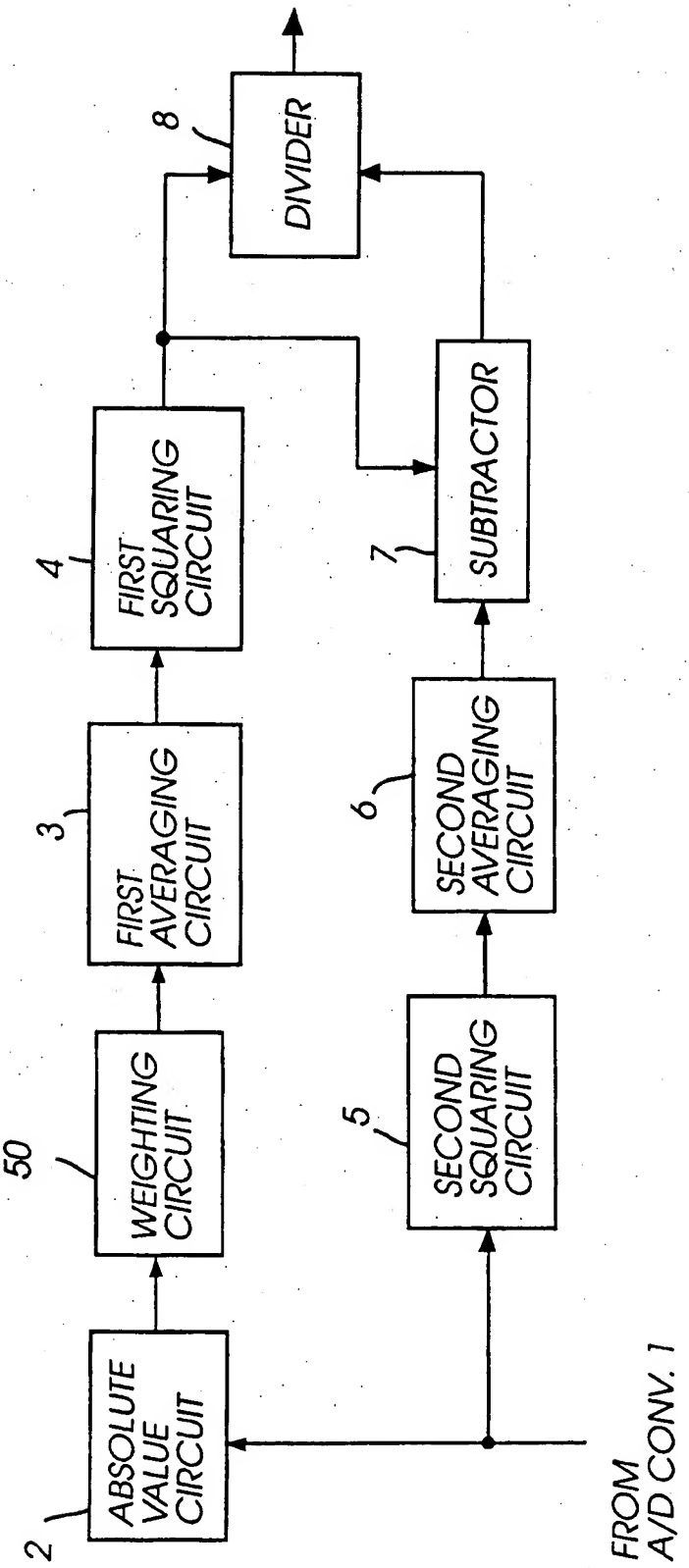

MEASURED VALUE
THEORETICAL VALUE (Eb/No(dB))
INPUT Eb/No(dB)
MEASURED VALUE
THEORETICAL VALUE
0
2
4
6
8
10
12
14
16
18
20

Fig. 10


ABSOLUTE VALUE CIRCUIT
2
WEIGHTING CIRCUIT
50
FIRST AVERAGING CIRCUIT
3
FIRST SQUARING CIRCUIT
4
SECOND SQUARING CIRCUIT
5
SECOND AVERAGING CIRCUIT
6
SUBTRACTOR
7
DIVIDER
8
FROM A/D CONV. 1

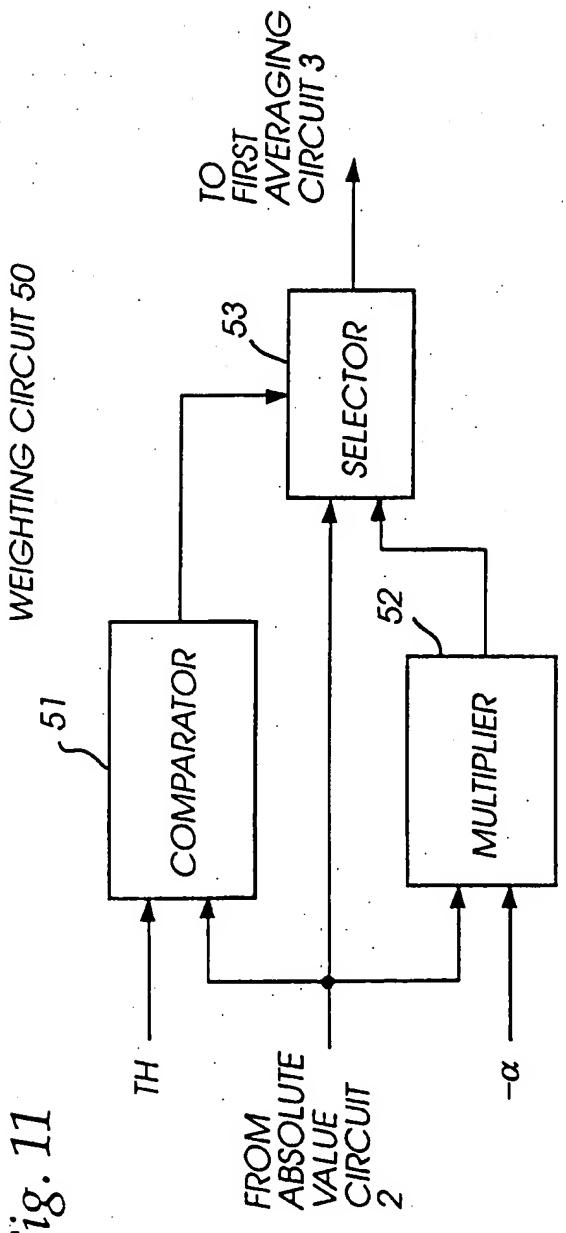


Fig. 11

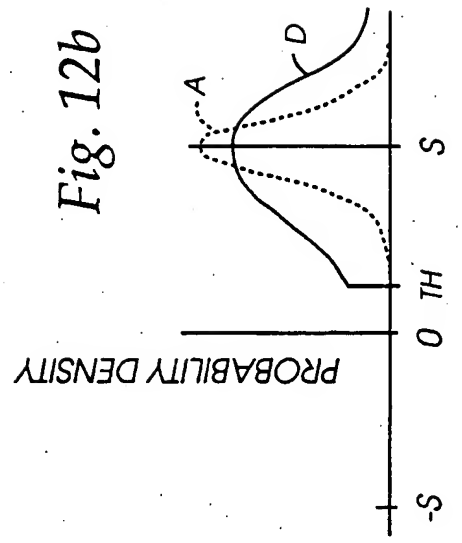


Fig. 12b

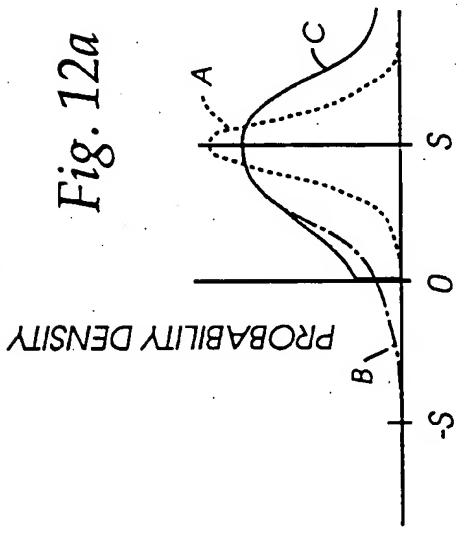


Fig. 12a

Fig. 13

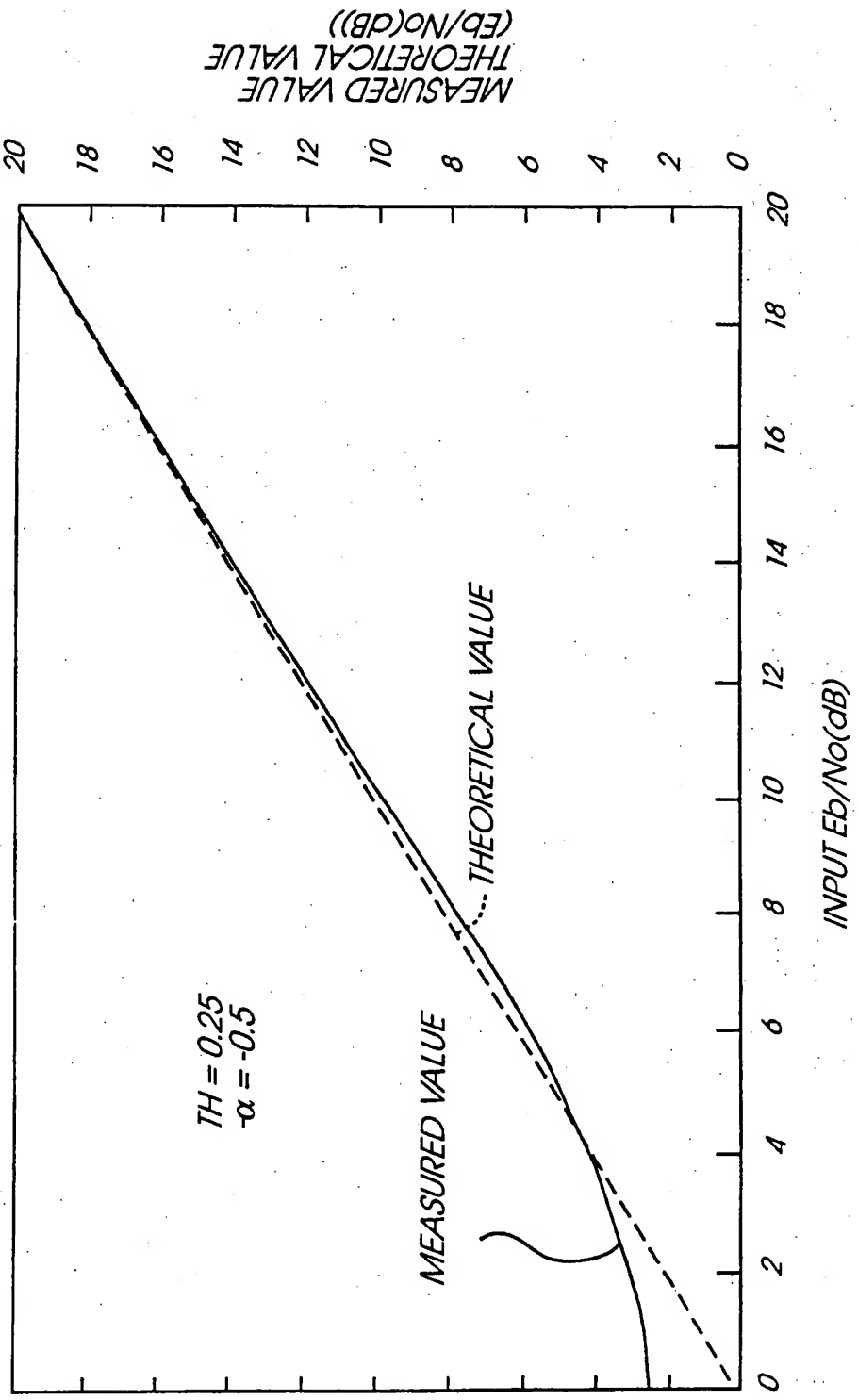
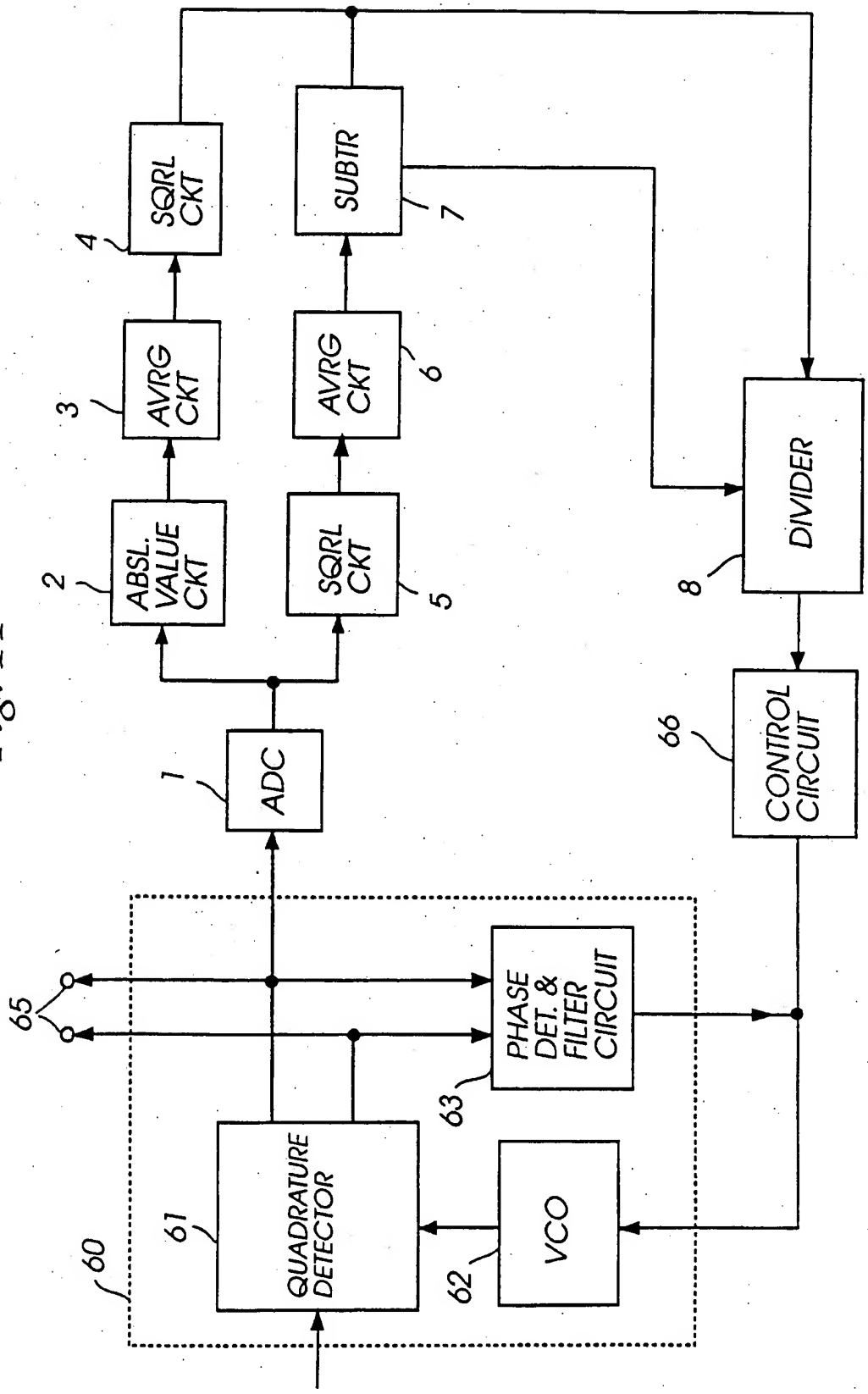

MEASURED VALUE
THEORETICAL VALUE
(Eb/No(dB))
THEORETICAL VALUE
MEASURED VALUE
TH = 0.25
α = -0.5
INPUT Eb/No(dB)
0
2
4
6
8
10
12
14
16
18
20

Fig. 14


ADC
1
ABSL. VALUE CKT
2
AVRG CKT
3
SQRL CKT
4
SQRL CKT
5
AVRG CKT
6
SUBTR
7
DIVIDER
8
CONTROL CIRCUIT
66
65
PHASE DET. & FILTER CIRCUIT
63
QUADRATURE DETECTOR
61
VCO
62
60